CLAIMS

WHAT IS CLAIMED IS:

1. A split-gate flash memory cell comprising:

an N-type well region formed in a substrate, the N-type well region having formed therein a P+ source, a P+ drain, and a channel region extending between the P+ source and the P+ drain;

a first insulating layer disposed over the well region;

a floating gate disposed over the first layer, wherein the floating gate is positioned over a first portion of the channel region but not a second portion of the channel region;

a second insulating layer disposed over the floating gate;

a control gate including a first portion disposed over the first insulating layer, the first portion of the control gate being positioned over the second portion of the channel region, the control gate including a second portion disposed over the second insulating layer; and

wherein the cell is operable to be programmed by a band-to-band hot electron (BBHE) technique and erased by a polysilicon-polysilicon tunneling technique.

2. The memory cell of claim 1, wherein the second insulating layer has a top wall portion disposed over the floating gate and a sidewall portion immediately adjacent to the floating gate.

3. The memory cell of claim 2, wherein the first portion of the control gate is positioned immediately adjacent to the sidewall portion of the second insulating layer, wherein the second portion of the control gate is disposed over the top wall portion of the second insulating layer to minimize capacitive coupling with the floating gate.

4. The memory cell of claim 1, wherein the channel region is a P-channel.

5. The memory cell of claim 1, wherein the floating gate includes a tip portion, the tip portion producing a stronger electric field compared to the memory cell without the tip.

6. The memory cell of claim 1, wherein the cell is operable by applying dual high voltages.

7. The memory cell of claim 1, wherein the cell is operable by applying single high voltages.

8. The memory cell of claim 1, wherein the P+ drain is coupled to a bit line of the cell.

9. The memory cell of claim 1, wherein the control gate is coupled to a word line of the cell.

10. A method for improving endurance characteristics of a flash memory cell, the method comprising:

defining the flash memory cell to include a split-gate, P-channel structure;

erasing the flash memory cell by a polysilicon-polysilicon tunneling technique; and

programming the flash memory cell by a band-to-band hot electron technique.

11. The method of claim 10, wherein the structure includes:

an N-type well region formed in a substrate, the N-type well region having formed therein a P+ source, a P+ drain, and a channel region extending between the P+ source and the P+ drain;

a first insulating layer disposed over the well region;

a floating gate disposed over the first layer, wherein the floating gate is positioned over a first portion of the channel region but not a second portion of the channel region;

a second insulating layer disposed over the floating gate;

a control gate including a first portion disposed over the first insulating layer, the first portion of the control gate being positioned over the second portion of the channel region, the control gate including a second portion disposed over the second insulating layer.

12. The method of claim 11, wherein the second insulating layer has a top wall portion disposed over the floating gate and a sidewall portion immediately adjacent to the floating gate.

13. The method of claim 11, wherein the first portion of the control gate is positioned immediately adjacent to the sidewall portion of the second insulating layer, wherein the second portion of the control gate is disposed over the top wall portion of the second insulating layer to minimize capacitive coupling with the floating gate.

14. The method of claim 11, wherein the channel region is a P-channel.

15. The method of claim 11, wherein the floating gate includes a tip portion, the tip portion producing a stronger electric field compared to the memory cell without the tip.

16. The method of claim 11, wherein the cell is operable by applying dual high voltages.

17. The method of claim 11, wherein the cell is operable by applying single high voltages.

18. The method of claim 11, wherein the P+ drain is coupled to a bit line of the cell.

19. The method of claim 11, wherein the control gate is coupled to a word line of the cell.